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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER
WANG, ALBERT C

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,294	NALAWADI ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-15,17-20,22-25 and 27-29* is/are rejected.

7)☒ Claim(s) *10,16,21 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive the amendment filed 4 August 2005.

2. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 22 recites the limitation "the hardware generated USB interrupts". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-4, 6-9, 12, 14, 15, 19, 24, 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi, U.S. Patent No. 6,615,288, in view of Wooten, U.S. Patent No. 6,272,499.

As per claim 1, Herzi teaches a system comprising:

a processor coupled to a bus (fig. 2, CPU 201);

a memory coupled to the bus (fig. 2, memory 203);

an external bus controller coupled to the bus (fig. 1, USB controller; col. 2, 24-35); and

a basic input-output system (BIOS) coupled to the bus (fig. 2, BIOS 202), the BIOS comprising an external bus support component to cause a interrupt to be generated and to provide support for external bus enabled devices responsive to the interrupt (figs. 3 & 4; col. 5, lines 36-52).

Even though Herzi does not expressly teach causing the interrupt to be generated periodically, Herzi's method is capable of doing so. Since Herzi's interrupt is generated in response to receiving input from an external bus device, the interrupt is generated periodically when inputs are received periodically from an external bus device. Wooten teaches periodically processing either isochronous transfers or interrupt transfers (col. 12, lines 37-45). Isochronous transfers are time-sensitive and need to be processed periodically; whereas interrupt transfers tend to occur at low frequency in bursts (col. 6, lines 5-22). Because Wooten teaches that a USB device with an interrupt endpoint is polled at a given frequency (col. 12, lines 46-50), interrupt transfers are also be processed periodically if during a burst, new data is available every 2^n time an interrupt endpoint is polled. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art that in view of Wooten's periodic data transfer, Herzi's method causes the interrupt to be generated periodically.

As per claim 2, Herzi teaches the external bus support component is to provide support for external bus enabled devices until an operating system providing external bus support is loaded (col. 1, line 66 – col. 2, line 20).

As per claim 3, Herzi teaches the system of claim 1 wherein the external bus enabled devices comprise at least one of a keyboard, a mouse, a floppy drive, a biometric device, a hard disk drive, a compact disk read-only memory (CD-ROM) player (fig. 2).

As per claim 4, Herzi teaches the system of claim 1 wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled devices are USB devices (claim 8).

As per claim 6, Herzi teaches the interrupt is a system management interrupt (fig. 3, step 303; fig. 5, step 505) and Wooten teaches 32-bit Intel Architecture (col. 4, lines 25-30).

As per claim 7, Wooten teaches the processor is compatible with 32-bit Intel Architecture (col. 4, lines 25-30).

As per claim 8, Herzi teaches a system comprising:

a processor coupled to a bus (fig. 2, CPU 201);

a memory coupled to the bus (fig. 2, memory 203);

an external bus controller coupled to the bus (fig. 1, USB controller; col. 2, 24-35);

an external bus enabled device coupled to the external bus controller (fig. 1, USB keyboard, USB mouse);

a basic input-output system (BIOS) coupled to the bus (fig. 2, BIOS 202), the BIOS having instructions which when executed cause the processor to perform operations comprising:

obtaining a portion of the memory to be used to maintain a plurality of external bus device data (col. 6, lines 16-33);

causing an interrupt to be generated (figs. 3 & 5); and

handling input produced by the external bus enabled device using the portion of the memory responsive to the interrupt (figs. 3 & 5).

Even though Herzi does not expressly teach causing the interrupt to be generated periodically, Herzi's method is capable of doing so. Since Herzi's interrupt is generated in response to receiving input from an external bus device, the interrupt is generated periodically when inputs are received periodically from an external bus device. Wooten teaches periodically processing either isochronous transfers or interrupt transfers (col. 12, lines 37-45). Isochronous transfers are time-sensitive and need to be processed periodically; whereas interrupt transfers tend to occur at low frequency in bursts (col. 6, lines 5-22). Because Wooten teaches that a USB device with an interrupt endpoint is polled at a given frequency (col. 12, lines 46-50), interrupt transfers are also be processed periodically if during a burst, new data is available every 2^n time an interrupt endpoint is polled. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art that in view of Wooten's periodic data transfer, Herzi's method causes the interrupt to be generated periodically.

Wooten teaches further:

obtaining a portion of a memory to be used to maintain a plurality of USB device data (col. 3, lines 54-64; col. 5, line 66 – col. 6, line 4; col. 6, lines 54-65); and

handling input produced by one or more USB devices using the portion of the memory (fig. 1, devices 132-136, 140-144 and 146-150 communicate via USB host controller 130; col. 5, lines 23-56; col. 11, lines 11-24; col. 12, lines 8-23).

As per claim 9, Herzi teaches the interrupt is a system management interrupt (fig. 3, step 303; fig. 5, step 505) and Wooten teaches 32-bit Intel Architecture (col. 4, lines 25-30).

As per claim 12, Herzi teaches the system of claim 8 wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled devices are USB devices (claim 8).

As per claim 14, Herzi teaches a method comprising:

causing an interrupt to be generated by an external bus support component (fig. 3, step 303; fig. 5, step 503; col. 5, lines 59 – col. 6, line 9; col. 7, lines 20-30); and

handling input produced by one or more USB devices (fig. 3, step 302 and 304; fig. 5, steps 502 and 505-509; col. 5, lines 59 – col. 6, line 9; col. 7, lines 20-30)

Even though Herzi does not expressly teach causing the interrupt to be generated periodically, Herzi's method is capable of doing so. Since Herzi's interrupt is generated in response to receiving input from an external bus device, the interrupt is generated periodically when inputs are received periodically from an external bus device. Wooten teaches periodically processing either isochronous transfers or interrupt transfers (col. 12, lines 37-45). Isochronous transfers are time-sensitive and need to be processed periodically; whereas interrupt transfers tend to occur at low frequency in bursts (col. 6, lines 5-22). Because Wooten teaches that a USB device with an interrupt endpoint is polled at a given frequency (col. 12, lines 46-50), interrupt transfers are also be processed periodically if during a burst, new data is available every 2^n time an interrupt endpoint is polled. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art that in view of Wooten's periodic data transfer, Herzi's method causes the interrupt to be generated periodically.

Wooten teaches further:

obtaining a portion of a memory to be used to maintain a plurality of USB device data (col. 3, lines 54-64; col. 5, line 66 – col. 6, line 4; col. 6, lines 54-65); and

handling input produced by one or more USB devices using the portion of the memory (fig. 1, devices 132-136, 140-144 and 146-150 communicate via USB host controller 130; col. 5, lines 23-56; col. 11, lines 11-24; col. 12, lines 8-23).

As per claim 15, Herzi teaches the interrupt is a system management interrupt (fig. 3, step 303; fig. 5, step 505) and Wooten teaches 32-bit Intel Architecture (col. 4, lines 25-30).

As per claim 19, Wooten teaches sending data to one or more USB devices using the portion of the memory (col. 6, lines 38-49).

As per claim 24, Herzi teaches a method comprising:

causing an interrupt to be generated by an external bus support component (fig. 3, step 303; fig. 5, step 503; col. 5, lines 59 – col. 6, line 9; col. 7, lines 20-30); and

handling input produced by one or more USB devices (fig. 3, step 302 and 304; fig. 5, steps 502 and 505-509; col. 5, lines 59 – col. 6, line 9; col. 7, lines 20-30)

Even though Herzi does not expressly teach causing the interrupt to be generated periodically, Herzi's method is capable of doing so. Since Herzi's interrupt is generated in response to receiving input from an external bus device, the interrupt is generated periodically when inputs are received periodically from an external bus device. Wooten teaches periodically processing either isochronous transfers or interrupt transfers (col. 12, lines 37-45). Isochronous transfers are time-sensitive and need to be processed periodically; whereas interrupt transfers tend to occur at low frequency in bursts (col. 6, lines 5-22). Because Wooten teaches that a USB

device with an interrupt endpoint is polled at a given frequency (col. 12, lines 46-50), interrupt transfers are also be processed periodically if during a burst, new data is available every 2^n time an interrupt endpoint is polled. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art that in view of Wooten's periodic data transfer, Herzi's method causes the interrupt to be generated periodically.

Wooten teaches further:

obtaining a portion of a memory to be used to maintain a plurality of USB device data (col. 3, lines 54-64; col. 5, line 66 – col. 6, line 4; col. 6, lines 54-65); and

handling input produced by one or more USB devices using the portion of the memory (fig. 1, devices 132-136, 140-144 and 146-150 communicate via USB host controller 130; col. 5, lines 23-56; col. 11, lines 11-24; col. 12, lines 8-23).

However, while Herzi teaches a BIOS firmware (fig. 2, BIOS 202), Herzi does not expressly teach a machine readable medium having instructions for the updating of BIOS to support the method steps above. Official Notice is taken that using a machine readable medium for "re-flashing" of flash ROM to provide an updated version of BIOS is well known in the art (for example see Gharda et al., U.S. Patent No. 6,560,702, col. 1, lines 53-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art that "re-flashing" is common practice for updating BIOS code.

As per claim 25, Herzi teaches the interrupt is a system management interrupt (fig. 3, step 303; fig. 5, step 505) and Wooten teaches 32-bit Intel Architecture (col. 4, lines 25-30).

As per claim 28, Herzi teaches the system of claim 8 wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled devices are USB devices (claim 8).

5. Claims 5, 13, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Wooten as applied to claims 1, 8, 14, and 24 above, and further in view of Intel, "Instantly Available Power Managed Desktop PC Design Guide", Revision 1.2, September 25, 1998 ("Intel").

As per claim 5, Herzi/Wooten does not expressly teach details of memory mapping and BIOS with regards to the ACPI specification and the BIOS comprises a software component to implement the ACPI specification. Intel teaches such details (sec. 4, ACPI BIOS design considerations). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Intel's ACPI implementation to Herzi/Chaiken's system. A motivation for doing so would have been to facilitate power management (Intel, sec. 1.1).

As per claims 13, 18, and 29, Intel teaches a non-volatile-sleeping (NVS) memory region (sec. 4.2.2, ACPI Non-Volatile-Sleeping Memory).

6. Claims 11, 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Wooten as applied to claims 8, 14, and 24 above, and further in view of Chaiken, U.S. Patent No. 6,128,732.

As per claims 11, 17 and 27, Chaiken teaches de-allocating a portion of memory when code in that portion is no longer needed, in order to leave space for software applications (col. 1, line 60 – col. 2, line 5). When an operating system providing external bus device support is

completely loaded, it is obvious that the code in the portion of memory is redundant, and is no longer needed.

7. Claim 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Wooten as applied to claim 14 above, and further in view of Eichler, Jr. et al., U.S. Patent No. 6,772,252 ("Eichler").

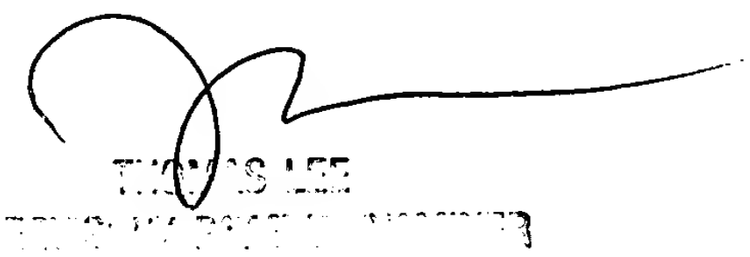
As per claim 20, Herzi/Wooten does not expressly teach determining whether an operating system providing USB device support is loaded. Eichler teaches determining whether an operating system provides USB support (fig. 7, step 704). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Eichler's determining to Herzi/Wooten's method. A motivation for doing so would have been to determine when code is no longer necessary.

8. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Wooten as applied to claim 14 above, and further in view of Gentry, Jr. et al., U.S. Patent No. 6,467,008 ("Gentry").

As per claim 23, Herzi/Wooten does not expressly teach adjusting the rate of the interrupt based on data traffic involving the one or more USB devices. Gentry teaches adjusting the rate of an interrupt based on data traffic (col. 7, line 51 – col. 8, line 11) involving one or more USB devices (col. 5, lines 53-65). At the time of the invention it would have been obvious to one of ordinary skill in the art to apply Gentry's interrupt modulation to Herzi/Wooten's method, in order to allow a processor to be more responsive to other tasks (Gentry, col. 7, lines 19-36).

Allowable Subject Matter

9. Claims 10, 16, 21 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.



THOMAS LEE